In the Specification

Please amend paragraph [0019] as follows:

[0019] Following are [[~~detail~~]]detailed descriptions of the step 140. Referring to FIG. 1 and 2, the step 141 determines timing between SyncFnd and SyncWin (which could be viewed as to determine where the SyncFnd is [[~~locate~~]]located in the SyncWin). If it is in the front-edge region unlockFront, the step 142 is performed. If it is in the frequency-lock region lockM, the step 143 is performed. If it is in the post-edge region unlockPost, the step 144 is performed. After a frequency-increase signal is sent out in step 142, the step 150 is performed. After a frequency-remain signal is sent out in step 143, the step 150 is performed. After a frequency-reduction signal is sent out in step 144, the step 150 is performed. The step 150 corrects the clock signal EFMCLK according to the frequency-increase signal, the frequency-reduction signal and the frequency-remain signal.

Please amend paragraph [0020] as follows:

[0002] Following are [[~~detail~~]]detailed descriptions of the step 150. Referring to FIG. 1, the step 151 measures and determines whether a number of the frequency-increase signal is larger than a preset counting number N1, wherein if it is, a frequency–increase trigger signal is generated and the number of the frequency-increase signal is reset. The step 152 measures and determines whether a number of the frequency-remain signal is larger than a preset counting number N2, wherein if it is, a frequency–remain trigger signal is generated and the number of the

frequency-reduction signal is reset. The step 153 measures and determines whether a number of the frequency-reduction signal is larger than a preset counting number N3, wherein if it is, a frequency–reduction trigger signal is generated and the number of the frequency-remain signal is reset. The step 154 corrects the clock signal EFMCLK according to the frequency-increase signal, the frequency-remain signal and the frequency-reduction signal. For example, the frequency-increase signal, the frequency-reduction signal and the frequency-remain signal are transmitted to a clock generator[[~~EFMCLK~~]]. Accordingly, the clock generator corrects the clock signal EFMCLK. The preset counting numbers N1, N2 and N3 can be the same counting number or different to each other, which means there is an elasticity to adjust.